|  |  |
| --- | --- |
| Name: | EE-272L Digital Systems Design |
| Reg. No.: | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual 4(a)**

**Combinational Circuit Design For RGB**

**Task1 (Truth Table):**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs Conditions Output** | | | | | | | | | |
| a0 | a1 | b0 | b1 | a<b | a>b | a=b | Red | Green | Blue |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |

**Task2 (K-Maps):**

Red: a0a1

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |

b0b1 00 01 11 10

R = a0a1 + b0`b1` + a1b0` + a0b0`+ a0b1`

Green:

a0a1

00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |

b0b1

G = a0`a1` + a0`b1 + a1`b0 + b0b1 + a0`b0

Blue:

a0a1

00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

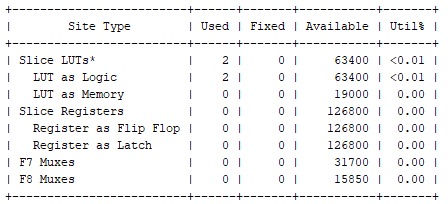
b0b1

B = a1`b1 + a1b1` + a0`b0 + a0b0`

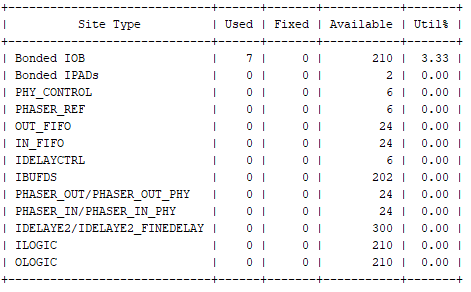
**Task3 (Verilog Code):**

* Separate page attached.

**Task4 (Resources):**

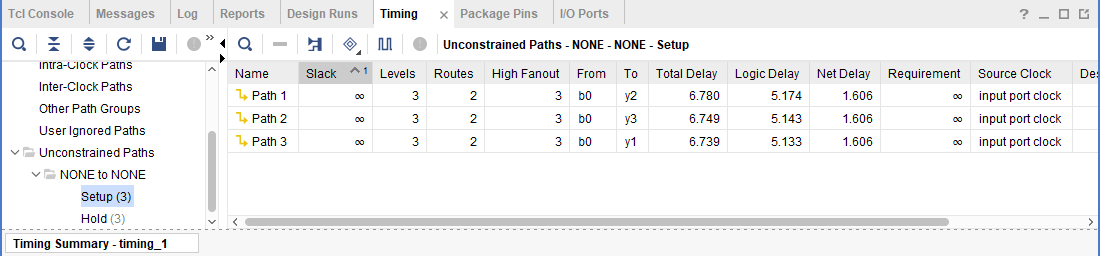


LUT Utilization

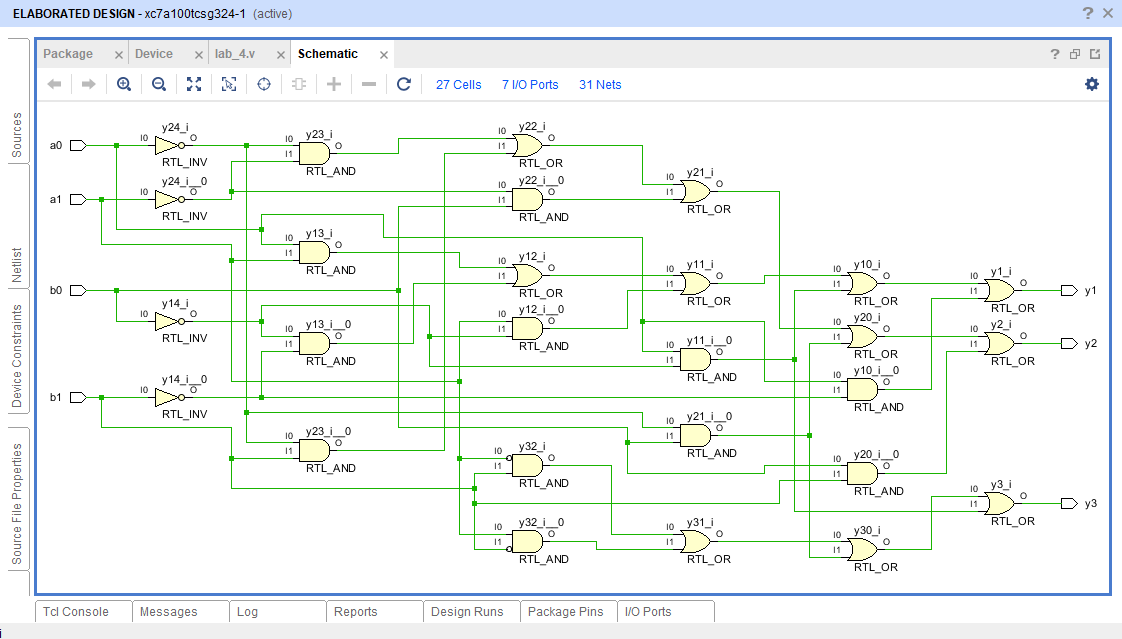


I/O Utilization

**Task5 (Maximum Combinational Delay):**



**Task6 (Schematic):**



**Task7 (Testbench Code):**

* Separate page attached.

**Task8 (Simulations):**

